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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No. 0756-1881

First Inventor or Application Identifier: Hongyong Zhang

Title: Semiconductor Device and Method for Fabricating the Same

Express Mail Label No.

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [x] Fee Transmittal Form (e.g , PTO/SB/17)
   (Submit an original, and a duplicate for fee processing)
2. [x] Specification *Total Pages* [32]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [x] Drawing(s) (35 USC 113) *Total Sheets* [7]
4. [x] Oath or Declaration *Total Pages* [2]
   a [ ] Newly executed (original or copy)
   b. [x] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [x] Incorporation By Reference *(useable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ADDRESS TO:

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Box Patent Application
Washington, DC 20231

6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
   (if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3 73(b) Statement [ ] Power of Attorney
   (when there is an assignee)
10. [ ] English Translation Document *(if applicable)*
11. [x] Information Disclosure Statement [ ] Copies of IDS
    (IDS)/PTO-1449 Citations
12. [x] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
    (Should be specifically itemized)
14. [ ] *Small Entity [ ] Statement filed in prior application,
    Statement(s) Status still proper and desired
    (PTO/SB/09-12)
15. [ ] Certified Copy of Priority Document(s)
    (if foreign priority is claimed)
16 [ ] Other

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.

17. **If a CONTINUING APPLICATION**, *check appropriate box, and supply the requisite information below and in a preliminary amendment*
    [ ] Continuation [x] Divisional [ ] Continuation-in-part (CIP) of prior application No. 08/908,204
    Prior application information: Examiner: V. Wallace Group/Art Unit:2815

18. CORRESPONDENCE ADDRESS

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Signature [signature] Date: 11-11-98

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Complete If Known	
Application Number	Based on USSN 08/908,204
Filing Date	Unassigned
First Named Inventor	Hongyong Zhang et al.
Examiner Name	V. Wallace
Group Art Unit	2815
Attorney Docket Number	0756-1881

TOTAL AMOUNT OF PAYMENT	($)1,388 00

METHOD OF PAYMENT (check one)

1. [x] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:
   Deposit Account No 19-2380(0756-1881)
   Deposit Account Name SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, PC

   [x] Charge Any Additional Fee Required Under 37 CFR 1 16 and 1 17

   [ ] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance

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FEE CALCULATION

1 BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	[ ]
106	330	206	165	Design filing fee	[ ]
107	540	207	270	Plant filing fee	[ ]
108	790	208	395	Reissue filing fee	[ ]
114	150	214	75	Provisional filing fee	[ ]
				SUBTOTAL (1)	[790]

2. EXTRA CLAIM FEES

	Extra Claims		Fee from Below		Fee Paid
Total Claims	36	- 20** =	16	X 22 =	$352 00
Independent Claims	6	- 3** =	3	X 82 =	$246 00
Multiple Dependent Claims				=	

**or number previously paid, if greater, For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim
109	82	209	41	**Reissue independent claims over original patent
110	22	210	11	**Reissue claims in excess of 20 and over original patent
				SUBTOTAL (2) [598]

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge-late filing fee or oath	
127	50	227	25	Surcharge-late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Ext for reply within first month	
116	400	216	200	Ext for reply within second mth	
117	950	217	475	Ext for reply within third mth	
118	1,510	218	755	Ext for reply within fourth mth	
128	2,060	228	1,030	Ext for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing brief in support of appeal	
121	270	221	135	Request for Oral Hearing	
138	1,510	138	1,510	Petition to institute public use proceeding	
140	110	240	55	Petition to revive-unavoidable	
141	1,320	241	660	Petition to revive-unintentional	
142	1,320	242	660	Utility issue fee (or reissue)	
143	450	243	225	Design issue fee	
144	670	244	335	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of IDS	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	790	246	395	Filing a submission after final rejection (37 CFR 1 129(a))	
149	790	249	395	For each additional invention to be examined (37 CFR 1 129(b))	
				Other	
				Other	
				*Reduced by Basic Filing Fee Paid	
				SUBTOTAL (3)	$

SUBMITTED BY

Complete (if applicable)	

Typed or Printed Name	Eric J. Robinson, Esquire			Reg. Number	38,285
Signature		Date	11-11-98	Deposit Account User ID	19-2380(0756-1881)

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SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an insulated gate thin film transistor formed on an insulating material (e.g., glass) or a material such as a silicon wafer having thereon an insulating film (e.g., silicon oxide), and to a method for fabricating the same. The present invention is particularly effective for thin film transistors fabricated on a glass substrate having a glass transition temperature (deformation temperature or deformation point) of 750 °C or less. The thin film transistor according to the present invention is useful for driver circuits of, for example, active matrix liquid crystal displays and image sensors, as well as for three dimensional integrated circuits.

2. Description of the Related Art

Thin film transistors (referred to simply hereinafter as " TFTs") are widely employed for driving, for example, liquid crystal displays of active matrix type and image sensors. TFTs of crystalline silicon having a higher electric field mobility are also developed as an alternative for amorphous silicon TFTs to obtain high speed operation. However, TFTs with further improved device characteristics and durability can be obtained by forming an impurity region having a high resistance (high resistance drain; HRD).

Fig. 4A shows a cross section view of a conventional TFT having an HRD. The active layer comprises low resistance regions 1 and 5, a channel forming region 3, and high resistance regions 2 and 4 formed therebetween. A gate insulating film 6 is provided to cover the active layer, and a gate electrode 7 is formed on the channel forming region 3 through the gate insulating film 6. An interlayer dielectric 8 is formed to cover the gate electrode 7, and source/drain electrodes 9 and 10 are connected to the low

resistance regions 1 and 5. At least one of the elements selected from oxygen, nitrogen, and carbon is introduced into the high resistance regions 2 and 4.

The introduction of at least one of the elements above, however, requires the use of photolithography. Thus, it is difficult to form high resistance regions on the edge portion of the gate electrode in a self-alignment; hence, the TFTs are fabricated at a low yield, and moreover, the TFTs thus obtained are not uniform in quality.

SUMMARY OF THE INVENTION

The present invention provides TFTs having uniform device characteristics at a high yield by forming the high resistance regions in a self-alignment without using photolithography.

A TFT according to the present invention is shown schematically in Fig. 4B. The position and the size of high resistance (impurity) regions 12 and 14 depend on a gate insulating film 16 and a gate electrode portion (comprising a gate electrode 17 and in some cases, an anodic oxide film 17'). That is, at least one of nitrogen, oxygen, carbon, etc., is introduced into the active layer using the gate electrode portion and the gate insulating film 16 as masks. By controlling the accelerating voltage of the ions to control the depth of ion doping, the ion concentration is found to be maximum at a predetermined depth. In case nitrogen ions are introduced at an accelerating voltage of 80 kV, a maximum concentration for nitrogen ions can be achieved at a depth of 1,000 Å. Even in an active layer, the concentration of nitrogen ions differs with the depth in such a case.

In case a gate insulating film and a gate electrode portion are provided at a thickness of 1,000 Å and 3,000 Å or more, respectively, the gate electrode portion is sufficiently thick to prevent nitrogen ions from introducing into the active layer formed under the gate electrode portion. As illustrated in Fig. 4C, most of the nitrogen ions pass through the active layer 21 at a portion

(shown with line B-B') where the active layer is exposed. Accordingly, nitrogen ions are found at a highest concentration at a portion under the active layer 21, e.g., the substrate. In contrast to this, a highest nitrogen ion concentration is achieved in the active layer at a portion (line A-A') where the gate electrode portion is not present and the gate insulating film 16 is present.

Accordingly, a high resistance region can be formed in a self-alignment by selectively introducing the nitrogen ions into the active layer under the portion at which the gate insulating film is present and the gate electrode portion is not present. Referring to Fig. 4D, low resistance (impurity) regions 11 and 15 and high resistance regions 12 and 14 are formed by doping an N- or P-type impurity. The N- or P-type impurity can be doped before introducing nitrogen ions.

In case of forming an anodic oxide 17' on the surface of the gate electrode 17, the high resistance regions 12 and 14 are offset from the gate electrode 17. The displacement x according to the offset depends on the thickness of the anodic oxide 17', and the low resistance regions 11 and 15 are displaced horizontally from the gate electrode 17 for a distance corresponding to the sum of the width of the region 12 and the displacement x.

According to the present invention, an oxide layer formed by anodically oxidizing the gate electrode and the like is used as the gate insulating film 16 to form the high resistance region in a self-alignment. The thickness of the anodic oxide can be precisely controlled. More specifically, the anodic oxide film can be formed uniformly at a thickness of 1,000 Å or less to a thickness of 5,000 Å or more (e.g., to 1 μm). Thus, this is preferred because a high resistance region can be formed with a greater degree of freedom, and, moreover, in case of using a self-aligned process, the high resistance region can be formed without causing fluctuation in its width.

In contrast to a so-called barrier type anodic oxide which is etched only by a hydrofluoric etchant, a porous type anodic oxide can be selectively etched by a phosphoric acid etchant and the like. Accordingly, an etching treatment can be effected without damaging other materials constituting the TFT, for example, silicon and silicon oxide. In case of dry etching, the barrier or porous anodic oxide is extremely resistant against etching, and exhibits a sufficiently high selectivity ratio in case of etching with respect to silicon oxide.

According to the present invention, a TFT can be fabricated by the following processes. Thus, high resistance regions can be formed with a higher certainty and therefore mass production is improved.

Referring to Figs. 1A to 1E, a basic process for fabricating a TFT according to the present invention is described below. A base insulating film 102 is formed on a substrate 101. An active layer 103 is formed from a crystalline semiconductor (a semiconductor comprising a crystal even at a small quantity, for example, a single crystal semiconductor, polycrystalline semiconductor, semi-amorphous semiconductor or the like is referred to as "a crystalline semiconductor" in the present invention. An insulating film 104 comprising silicon oxide is formed to cover an active layer 103, and a coating is formed by an anodically oxidizable material. Preferably, an anodically oxidizable material such as aluminum, tantalum, titanium, and silicon, is used as the coating material. Moreover, a monolayered gate electrode using one of the above materials as well as a multilayered gate electrode comprising two layers or more of the above materials can be utilized. For example, a double layered structure comprising titanium silicide formed on aluminum or a double layered structure comprising aluminum formed on titanium nitride can be used. Each of the layers is provided at a thickness depending on the device characteristics.

A mask film used as the mask in the anodic oxidation is formed to cover the coating and then the coating and the mask film are patterned and etched simultaneously, thereby to form a gate electrode 105 and a mask film 106. The mask film can be formed using a photoresist used in an ordinary photolithography process, a photosensitive polyimide, or a general etchable polyimide. (Fig.1A)

A porous anodic oxide 107 is formed on both sides of the gate electrode 105 by applying an electric current to the gate electrode 105 in the electrolytic solution. The anodic oxidation is effected using an aqueous acidic solution containing from 3 to 20 % of citric acid, nitric acid, phosphoric acid, chromic acid, sulfuric acid, and the like. An anodic oxide from 0.3 to 25 μm in thickness, more specifically, 0.5 μm in thickness, is formed by applying a voltage of about 10 to 30 V. The mask film 106 is removed by etching after the anodic oxidation. (Fig. 1B)

A barrier anodic oxide 108 can be formed on both sides and the upper surface of the gate electrode 105 by applying a current thereto in an ethylene glycol solution containing from 3 to 10 % of tartaric acid, boric acid, or nitric acid. The thickness of the anodic oxide thus formed depend on the voltage applied between the gate electrode 105 and the electrode face thereto.

The barrier anodic oxide is formed after forming the porous anodic oxide. The barrier anodic oxide 108 is formed not on the outer side of the porous anodic oxide 107, but between the porous anodic oxide 107 and the gate electrode 105. The etching rate of a phosphoric acid etchant to a porous anodic oxide is 10 times or more higher with respect to that to a barrier anodic oxide. Accordingly, the gate electrode 105 is protected from a phosphoric acid etchant because the barrier anodic oxide 108 remains substantially unetched in a phosphoric acid etchant (Fig. 1C).

The insulating film 104 is etched by dry etching, wet etching or the like. The etching can be effected until the active layer is exposed, or it may be stopped in the intermediate state.

Preferably from the viewpoint of mass production, yield, and the uniformity of the film, the insulating film is completely etched until the active layer is exposed. The thickness of the gate insulating film covered by the anodic oxide 107 and the gate electrode 105 remains unchanged during the etching. In case dry etching using a fluorine-based gas (e.g., NF_3 or SF_6) is effected on a gate electrode 105 containing mainly aluminum, tantalum, and titanium as well on an insulating film 104 containing mainly silicon oxide, the insulating film 104 made of a silicon oxide can be etched rapidly. Since the etching rate is sufficiently low for aluminum oxide, tantalum oxide, and titanium oxide, the insulating film 104 can be etched selectively. The insulating film 104 can be etched rapidly and selectively by wet etching using a hydrofluoric acid based etchant such as hydrofluoric acid diluted to 1/100 (Fig. 1D).

The anodic oxide 107 is removed thereafter. A phosphoric acid based aqueous solution, such as a mixed acid of phosphoric acid, acetic acid, and nitric acid, is preferred as the etchant.

Thus, a part of the insulating film 104 (referred to hereinafter as "gate insulating film") can be remained. A gate insulating film 104' is present under the gate electrode 105 and the barrier anodic oxide 108, as well as under the porous anodic oxide 107 to a position extended for a distance *y* from the edge portion of the barrier anodic oxide 108. The distance *y* is determined in a self-alignment. Accordingly, a region of the active layer 103 on which the gate insulating film 104' is formed and a region on which the gate insulating film 104' is not formed are for med in a self-alignment. A high resistance region containing the ions at a high concentration is formed in a self-alignment with respect to the gate electrode by introducing ions such as nitrogen, oxygen, and carbon into the active layer.

The distance *x* between the edge portion of the gate electrode and the edge portion of the source or the drain region

(see Fig. 4D) corresponds to the offset width, and the width of the high resistance region is controlled in a self-alignment by the distance y. Referring to Figs. 1D and 2C, the edge portion 109 of the gate insulating film 104' coincides approximately with the edge portion 121 of the high resistance portion 112. The high resistance region in a conventional technology is formed in a non-self-alignme nt. Accordingly, it is difficult to form the high resistance region and the gate electrode at the same position for all the TFTs on the same substrate. In the present invention, however, the width of the anodic oxide 107 can be precisely controlled by the applied current (charge) for anodic oxide.

The offset width between the gate electrode and the high resistance region can be set arbitrary by controlling the thickness of the anodic oxide 108. In general, the ON/OFF ratio increases as the reverse leak current reduces in an offset state. Thus, the TFT according to the present invention is suitable for a pixel TFT for controlling the pixels of an active matrix liquid crystal display in which a low leak current is required. However, since the hot carriers generated at the edge portions of the high resistance region are trapped by the anodic oxide, the characteristics of the TFT deteriorate.

In case of a TFT having a small offset, the deterioration of the TFT characteristics due to the trapping of hot carriers reduces and the ON current increases, but the leak current reversely increases. Accordingly, a TFT having a small offset is suitable for a TFT in which a large current drive capacity is required, for example, a driver TFT utilized in the peripheral circuits of monolithic active matrices. In practice, the TFT offset is determined by the usage of the TFT.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1E are a diagram showing the basic processes for fabricating a device according to the present invention;

Figs. 2A to 2C are a diagram showing the processes for fabricating a TFT according to Example 1 of the present invention;

Figs. 3A to 3C are a diagram showing the processes for fabricating a TFT according to Example 2 of the present invention;

Figs. 4A to 4D are a diagram showing the structure of TFTs according to the present invention;

Figs. 5A to 5F are a diagram showing the processes for fabricating a TFT according to Example 3 of the present invention;

Figs. 6A to 6F are a diagram showing the processes for fabricating a TFT according to Example 4 of the present invention;

Figs. 7A to 7F are a diagram showing the processes for fabricating a TFT according to Example 5 of the present invention; and

Figs. 8A and 8B are each integrated circuits of TFTs fabricated in Examples 1 and 3 according to the present invention, accordingly.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

EXAMPLE 1

A silicon oxide film having a thickness of 1,000 to 3,000 Å is formed as a base oxide film 102 on a Corning 7059 substrate 101 (300 x 400 mm or 100 x 100 mm in size) by sputtering in an oxygen atmosphere. For mass production, the film is deposited by decomposing TEOS using plasma CVD. A mono-layered film of aluminum nitride or a multilayered film of silicon oxide and aluminum nitride can be used as the base oxide film. The aluminum nitride film is formed by reactive sputtering in a nitrogen atmosphere.

An amorphous silicon film is deposited thereafter at a thickness of 300 to 5,000 Å, preferably, 500 to 1,000 Å, by plasma CVD or LPCVD, and is crystallized thereafter by allowing it to stand still in a reduction atmosphere in a temperature range of 550 to 600°C for 24 hours. The crystallization may be effected by laser irradiation. Thus crystallized silicon film is patterned to form an island-like region 103. A silicon oxide film 104 having a thickness

of 700 to 1,500 Å is formed by sputtering on the island-like region 103.

An aluminum film having a thickness of 1,000 Å to 3 μm and containing 1% by weight of silicon or 0.1 to 0.3% by weight of scandium (Sc) is formed thereafter by electron beam deposition or sputtering. Then, a photoresist (for example, OFPR 800/30cp, a product of Tokyo Ohka Co., Ltd.) is formed by spin coating. The photoresist can be formed with further improved adhesion strength by forming an aluminum oxide film having a thickness of 100 to 1,000 Å by anodic oxidation on the surface of the aluminum film before formation of the photoresist. The aluminum oxide film thus formed is effective in that it prevents current leakage from occurring from the photoresist, and in that it forms a porous anodic oxide only on the sides at anodic oxidation processing. The photoresist and the aluminum film are then patterned and etched to form a gate electrode 105 and a mask film 106 (Fig. 1A).

A porous anodic oxide 107 is formed at a thickness of 3,000 Å to 2 μm (for example, 5,000 Å), by anodic oxidation for 20 to 40 minutes, under a voltage of 10 to 30 V, specifically in this case, 10 V, in an aqueous acidic solution containing 3 to 20 % of, for example, citric acid, nitric acid, phosphoric acid, and sulfuric acid. An aqueous oxalic acid solution at 30 °C is used in the present example. The thickness of the anodic oxide can be controlled by the duration of anodic oxidation (Fig. 1B).

A mask film 106 is removed thereafter, and a voltage is applied to the gate electrode 105 in an electrolytic solution (i.e., an ethylene glycol solution containing from 3 to 10 % of tartaric acid, boric acid, or nitric acid) to form a barrier anodic oxide 108 on the upper portion and both sides of the gate electrode. In a case wherein a solution is at about 10 °C, an oxide film having a higher quality can be formed by the temperature to be lower than the room temperature. The thickness of the anodic oxide 108 thus formed increases in proportion to the applied voltage. In

case a voltage of 150 V is applied, an anodic oxide having a thickness of 2,000 Å is formed. The thickness of the anodic oxide 108 is determined by the required thickness and the degree of overlap. An anodic oxide having a thickness of 3,000 Å or more can be obtained by applying a voltage of 250 V or higher. However, in general, an anodic oxide film having a thickness of 3,000 Å or less is used because the application of such a high voltage impairs the TFT characteristics. Thus, the anodic oxidation is effected by applying a voltage of 80 to 150 V depending on the thickness required for the anodic oxide film 108 (Fig. 1C).

The silicon oxide film 104 is then etched by dry etching. The etching includes an isotropic etching in plasma mode and an anisotropic etching in reactive ion etching mode. The key is to set the selectivity ratio of silicon to silicon oxide to a sufficiently high value, and not to deeply etch the active layer. For example, the silicon oxide 104 alone can be etched while leaving the anodic oxide unetched by using CF_4 as the etching gas. The silicon oxide film 104' formed under the porous anodic oxide 107 is not etched in this process (Fig. 1D).

The anodic oxide 107 is etched using a mixed acid of phosphoric acid, acetic acid and nitric acid. The anodic oxide 107 alone is etched at a rate of about 600 Å/minute in this etching. The gate insulating film 104' remains unetched (Fig. 1E).

Nitrogen ions are then doped (introduced) into the active layer 103 at a dose of 1×10^{14} to 3×10^{16} cm^{-2}, for example, 2×10^{15} cm^{-2}, at an accelerating voltage of 50 to 100 kV, for example, at 80 kV, in a self-alignment by using the gate electrode portion (the gate electrode and the anodic oxide film at its periphery) and the gate insulating film as masks. Almost no nitrogen ions are introduced into the regions 110 and 113 on which the gate insulating film 104' is not formed. According to SIMS (secondary ion mass spectroscopy), the concentration of nitrogen in the regions 110 and 113 is 1×10^{19} atoms·cm^{-3} or less. On the other

hand, nitrogen atoms are introduced into the regions 111 and 112 on which the gate insulating film is formed at a concentration of 5 x 10^{19} to 2 x 10^{21} atoms·cm^{-3} depending on the depth (Fig. 2A).

Subsequently, an N-type impurity is introduced into the active layer at a dose of 5 x 10^{14} to 5 x 10^{15} cm^{-2} at an accelerating energy of 10 to 30 keV. By thus setting the accelerating energy to a low value, the N-type impurity can be excluded from the regions 111 and 112 because the gate insulating film functions as a barrier, but it can be introduced into the regions 110 and 113 at a sufficiently high quantity. The low resistance regions (source/drain regions) 114 and 117 and the high resistance regions 115 and 116 are formed in this manner by difference of the concentration of the N-type impurity and the nitrogen ions. Phosphine (PH_3) is used as the doping gas. Diborane (B_2H_6) can be used for forming a P-type impurity region (Fig. 2B).

The impurity ions and the nitrogen ions introduced into the active layer are activated thereafter by irradiating a laser radiation using a KrF excimer laser (a wavelength of 248 nm and a pulse width of 20 ns).

The impurity concentration in the regions 114 and 117 determined by SIMS is 1 x 10^{20} to 2 x 10^{21} atoms·cm^{-3}, and that in the regions 115 and 116 is 1 x 10^{17} to 2 x 10^{18} atoms·cm^{-3}. The dose for the former and the latter is 5 x 10^{14} to 5 x 10^{15} cm^{-2} and 2 x 10^{13} to 5 x 10^{14} cm^{-2}, respectively. The difference depends on whether there is a gate insulating film 104' or not. In general, the impurity concentration in the low resistance region is higher than that of the high resistance region by 0.5 to 3 digits.

Finally, a silicon oxide film is deposited by CVD at a thickness of 2,000 Å to 1 μm, for example, 3,000 Å as an interlayer dielectric 118. After forming the contact hole, the aluminum interconnection-electrodes 119 and 120 are formed. The resulting structure is then subjected to hydrogen annealing at 200 to 400 °C to obtain a TFT (Fig. 2C).

A process for fabricating a plurality of TFTs on the same substrate as shown in Fig. 8A is described according to the processes with reference to Figs. 1A to 1E and Figs. 2A to 2C. Fig. 8A shows an example in which a matrix region and a peripheral driver circuit for driving the matrix region are formed monolithically on the same substrate for an active matrix electro-optical device such as a liquid crystal display.

Referring to Fig. 8A, TFT1 and TFT2 are both driver TFTs. Anodic oxide films 501 and 502 are formed with a thickness of 200 to 2,000 Å, for example, 1,000 Å. In the structure, the high resistance region slightly overlaps with the gate electrode due to the impurity ions which diffuse upon ion doping. The drain of the N-channel TFT1 and that of the P-channel TFT2 are connected with each other with an interconnection 510. Although not shown in the figure, the source of the TFT1 is grounded and the source of the TFT2 is connected to the power source to establish a CMOS invertor.

TFT3 is a pixel TFT. An anodic oxide 503 is provided at a thickness of 1,000 Å. However, the high resistance region between the drain region and the gate electrode is provided with a width of 0.4 to 2 μm, for example, 0.5 μm, in order to reduce a leak current. The width of the high resistance region in TFT1 and TFT2 is, for example, 0.2 μm. The width of the high resistance region changes according to the thickness of the porous anodic oxide. Accordingly, the gate interconnection for the TFT1 and TFT2 is separated from that for the TFT3 so as to be controlled independently from each other. Furthermore, since the width of the high resistance region in TFT3 is large, the parasitic capacitance between the gate and drain which generates upon applying a voltage can be reduced.

EXAMPLE 2

A base film 102, an active layer 103, a gate insulating film 104', a gate electrode 105, and an anodic oxide 108 are formed

on a glass substrate 101 by processes similar to that described in Example 1 (Fig. 1E).

Nitrogen ions are introduced in a self-alignment into the active layer 103 using the gate electrode and the gate insulating film as masks. The dose is 1 x 10^{14} to 3 x 10^{15} cm^{-2}, for example, 2 x 10^{15} cm^{-2}. An accelerating voltage is 50 to 100 kV, for example, 80 kV. As a result, almost no nitrogen atoms are introduced into the regions 130 and 133 (the concentration of nitrogen is 1 x 10^{19} atoms·cm^{-3} or less in SIMS), but nitrogen atoms are introduced into the regions 131 and 132 at a concentration of 5 x 10^{19} to 2 x 10^{21} atoms·cm^{-3} depending on the depth (Fig. 3A).

The gate insulating film 104' is etched thereafter to form a gate insulating film 104" by using the anodic oxide 108 as a mask. An N-type impurity is introduced into the active layer thereafter by ion doping at a dose of 5 x 10^{14} to 5 x 10^{15} cm^{-2} and with an accelerating energy of 10 to 30 keV. Phosphine (PH_3) is used as the doping gas, but diborane (B_2H_6) can be used in case of forming a P-type impurity region. Thus impurity regions 134, 135, 136, and 137 are formed by introducing the N-type impurity at the same quantity to each of the regions 130, 131, 132, and 133. Depending on the quantity of the previously introduced nitrogen ions, the regions 134 and 137 become low resistance regions whereas the regions 134 and 136 become high resistance regions (Fig. 3B).

The impurity ions and the nitrogen ions introduced into the active layer are activated thereafter by irradiating a laser radiation using a KrF excimer laser (a wavelength of 248 nm and a pulse width of 20 ns). The impurity concentration in the regions 134, 135, 136, and 137 according to SIMS is 1 x 10^{20} to 2 x 10^{21} atoms·cm^{-3}, and the dose is 5 x 10^{14} to 5 x 10^{15} cm^{-2}.

Finally, a silicon oxide film is deposited by CVD at a thickness of 3,000 Å as an interlayer dielectric 138. After forming the contact hole, an aluminum interconnection-electrodes139 and 140

are formed. The resulting structure is then subjected to hydrogen annealing at 200 to 400 °C to obtain a TFT (Fig. 3C).

EXAMPLE 3

Referring to Figs. 5A to 5F, a method for fabricating an N-channel TFT is described below. First referring to the processes shown in Figs. 1A and 1B, a base oxide film 202, an island-like semiconductor (e.g., a crystalline silicon semiconductor) region 203, a silicon oxide film 204, and a gate electrode 205 comprising an aluminum film (200 nm to 1 μm in thickness) are formed on a substrate 201 having an insulating surface (e.g., a Corning 7059 glass), and a porous anodic oxide 206 (3,000 Å to 1 μm in thickness, e.g., 5,000 Å) is formed in both sides of the gate electrode 205 (Fig. 5A).

A barrier anodic oxide 207 (1,000 to 2,500 Å in thickness) is formed thereafter in the same manner as in the process described in Example 1 (Fig. 5B).

The silicon oxide film 204 is etched using the anodic oxide 206 as the mask, to form a gate insulating film 204'. Then, the anodic oxide film 206 is removed by etching using the anodic oxide film 207 as the mask. Impurity (phosphorus) is introduced by ion doping thereafter using the gate electrode 205, the film 207 and the gate insulting film 204' as the masks, to form low resistance regions 208 and 211 and the high resistance regions 209 and 210. The dose is 1 x 10^{14} to 5 x 10^{14} cm^{-2} and an accelerating voltage is 30 to 90 kV. Nitrogen ions are introduced after introducing the impurity ions at a dose of 1 x 10^{14} to 3 x 10^{16} cm^{-2}, more specifically, 2 x 10^{15} cm^{-2}, and an accelerating voltage is 50 to 100 kV, for example, 80 kV. As a result, almost no nitrogen is introduced into the low resistance regions 208 and 211, but nitrogen are introduced into the high resistance regions 209 and 210 at a concentration of 5 x 10^{19} to 2 x 10^{21} atoms·cm^{-3} depending on the depth (Fig. 5C).

Furthermore, a metallic coating (for example, a coating of titanium, nickel, molybdenum, tungsten, platinum, or palladium), specifically, for example, titanium layer 212 is deposited by sputtering at a thickness of 50 to 500 Å, to establish a tight adhesion with the low resistance regions 208 and 211 (Fig. 5D).

A laser radiation is irradiated using a KrF excimer laser (a wavelength of 248 nm and a pulse width of 20 ns) to activate the thus introduced impurities and to form metal silicide (titanium silicide) regions 213 and 214 by allowing the titanium film to react with silicon in the active layer. The energy density is 200 to 400 mJ/cm^2, preferably, 250 to 300 mJ/cm^2. Preferably, the substrate is heated at 200 to 500 °C upon irradiating the laser to prevent the titanium film from peeling. The laser does not need to be limited to an excimer laser, and other lasers are also usable. However, the use of a pulsed laser is preferred, because a continuous oscillated laser is irradiated for an excessively long duration, thereby to expand the object by heating and to cause film peeling.

An infrared laser such as an Nd:YAG laser (preferably, a Q-switch pulse oscillated laser), a visible light such as a second harmonic of the infrared laser, or various kinds of ultraviolet (UV) laser such as a KrF, a XeCl, an ArF, or the like excimer laser can be used as the pulse laser. However, a laser having a wavelength not reflected from a metallic film must be selected in a case wherein a laser is irradiated through the metallic film. In case the metallic film is very thin, any type of the lasers above can be used without any problem. In case the laser is irradiated through the substrate, a laser transmitted through a silicon semiconductor film must be selected.

Furthermore, lamp annealing using a visible light or a near infrared light may be employed in place of the aforementioned laser annealing. In lamp annealing, the duration of irradiation is controlled as such that the temperature of the light-irradiated

surface is about 600 to 1,000 °C. The duration of irradiation is, for example, several minutes at 600 °C, and several tens seconds at 1,000 °C. When the annealing is effected using a near infrared ray (specifically, for example, an infrared ray having a wavelength of 1.2 μm), the silicon semiconductor selectively absorbs the near infrared ray. Accordingly, the annealing can be effected without considerably heating the glass substrate. Moreover, the heating of the glass substrate can be suppressed by reducing the duration of irradiation per time.

Subsequently, the titanium film is etched using an etching solution containing a 5:2:2 mixture of hydrogen peroxide, ammonia, and water. The metal silicide regions 213 and 214 remain unetched (Fig. 5E).

Referring to Fig. 5F, a silicon oxide film is deposited as an interlayer dielectric 217 at a thickness of 2,000 Å to 1 μm, for example, 3,000 Å. After forming a contact hole, an aluminum interconnection-electrodes 218 and 219 are formed at a thickness of 2,000 Å to 1 μm, for example, 5,000 Å. The portion which the aluminum interconnection is in contact with is made of titanium silicide. Since the interface between aluminum and titanium silicide is stabler than that between aluminum and silicon, a highly reliable contact can be obtained. The reliability of the contact can be further improved by forming titanium nitride and the like as a barrier metal between the metal silicide regions 213 and 214 and the aluminum interconnection-electrodes 218 and 219. The sheet resistance of the titanium silicide region is 10 to 50 Ω/square. The sheet resistance of the high resistance regions 209 and 210 which have the same conductivity type as that of source/drain is 10 to 500 kΩ/square.

In the present example, the low resistance region 211 can be coincided approximately with the metal silicide region. The edge portion 215 of the gate insulating film 204' can be roughly coincided with the boundary 216 between the high resistance region

210 and the low resistance region 211, and the edge portion 215 can be coincided with nearly the edge portion of the metal silicide region 214.

A method for fabricating a plurality of TFTs on the same substrate as shown in Fig. 8B is described with reference to Figs. 5A to 5F. Fig.8B shows an example in which a matrix region and a peripheral driver circuit for driving the matrix region are formed monolithically on the same substrate for an active matrix electro-optical device such as a liquid crystal display. TFT1 and TFT2 utilized as the driver TFTs are formed in a CMOS invertor structure. The anodic oxide 505 and 506 are formed at a thickness of 200 to 2,000 Å, for example, 1,000 Å. TFT3 is a pixel TFT, and comprises a 1,000 Å thick anodic oxide 507.

The thickness of the anodic oxide is selected in such a manner that the edge portions of the gate electrode be coincided with the edge portions of the source and drain regions by taking the diffusion which occurs upon ion doping into account. One of the source and drain electrodes for TFT3 is connected to the ITO pixel electrode 508. The high resistance region for the TFT3 is formed at a width *ya'* of 0.4 to 5 μm, for example, *ya'* of 0.5 μm, while the high resistance regions for the TFT1 and TFT2 is provided, for example, at a width *ya* of 0.2 μm. Since the width of the high resistance region changes in accordance with the thickness of the porous anodic oxide, the interconnection at anodic oxidation is set in a separate series so that the interconnection for the TFT1 and TFT2 can be controlled independently from that for TFT3. The TFT1 and the TFT3 are each an N-channel TFT, while the TFT2 is a P-channel TFT. The parasitic capacitance between the gate and drain which generates upon applying a voltage can be thus reduced by the high resistance region for TFT3 provided at a large width.

In the present Example, a titanium film is deposited after ion doping. However, doping can be effected after depositing the titanium film. Because the entire surface is coated with a titanium

film upon irradiating the ion, an abnormal charging up which is often generated in use for an insulated substrate, can be prevented from occurring. Otherwise, annealing using a laser and the like is performed after ion doping, and then titanium silicide can be formed after forming the titanium film by irradiating a laser radiation and the like or by thermal annealing.

EXAMPLE 4

Referring to Figs. 6A to 6F, the present invention is described below. First referring to the processes shown in Figs. 1A to 1C, a base oxide film 302, an island-like semiconductor (e.g., a silicon semiconductor) region 303, a silicon oxide film 304, and a gate electrode 305 comprising an aluminum film (2,000 Å to 1 μm in thickness) are formed on a substrate 301 having an insulating surface (e.g., a Corning 7059). A porous anodic oxide 306 having a thickness of 6,000 Å is formed in both sides of the gate electrode. Furthermore, a barrier anodic oxide 307 is formed between the gate electrode 305 and the anodic oxide 306 (Fig. 6A).

The silicon oxide film 304 is etched using the anodic oxide 306 as the mask, to form a gate insulating film 304'. Then, the anodic oxide 306 is etched to expose a part of the gate insulating film 304'. A metallic film 308, for example, a titanium film (50 to 500 Å in thickness) is formed by sputtering (Fig. 6B).

Oxygen ions are introduced in a self-alignment into the active layer 303 using the gate electrode portion and the gate insulating film as the masks. The dose is 1 x 10^{14} to 3 x 10^{16} cm^{-2}, for example, 2 x 10^{15} cm^{-2}, and an accelerating voltage is 50 to 100 kV, for example, 80 kV. As a result, almost no oxygen is introduced into the regions 309 and 312 (the concentration of oxygen is 1 x 10^{19} atoms·cm^{-3} or less in SIMS), but the oxygen is introduced into the regions 310 and 311 at a concentration of 5 x 10^{19} to 2 x 10^{21} atoms·cm^{-3} depending on the depth (Fig. 6C).

An N-type impurity is introduced into the active layer thereafter by ion doping at a dose of 5 x 10^{14} to 5 x 10^{15} cm^{-2} and

with an accelerating energy of 10 to 30 keV. By thus setting the accelerating voltage to a low value, the N-type impurity can be mostly excluded from the regions 310 and 311 because the gate insulating film functions as a barrier, but it can be introduced into the regions 309 and 312 at a sufficiently high quantity. The low resistance regions (source/drain regions) 313 and 316 and the high resistance regions 314 and 315 are formed by difference of the concentration of the N-type impurity and the oxygen ions. Phosphine (PH_3) is used as the doping gas. Diborane (B_2H_5) can be used for forming a P-type impurity region (Fig.6D).

A KrF excimer laser (a wavelength of 248 nm and a pulse width of 20 ns) is irradiated to activate the impurities thus introduced into the regions 314 and 315 and to form metal silicide (titanium silicide) regions 317 and 318 by reaction of the titanium film and silicon in the active layer. The energy density is 200 to 400 mJ/cm^2, preferably, 250 to 300 mJ/cm^2. Preferably, the substrate is heated at 200 to 500 °C upon irradiating the laser to prevent the titanium film from peeling. Otherwise, lamp annealing by the irradiation of a visible light or a near infrared light can be effected (Fig. 6E).

Subsequently, the titanium film is etched using an etching solution containing a 5:2:2 mixture of hydrogen peroxide, ammonia, and water. The regions 317 and 318 remain unetched, while the gate insulating film 304' is etched using the gates 305 and 307 as the masks, to prevent the structure from being influenced by the impurities introduced into the gate insulating film 304'. Thus a gate insulating film 304" formed under the gate electrode portion remains.

As shown in Fig. 6F, a silicon oxide film is formed by CVD at a thickness of 6,000 Å as an interlayer dielectric 319. An aluminum interconnection-electrodes 320 and 321 are formed after forming the contact hole to complete a TFT having a high resistance region.

EXAMPLE 5

In Fig. 7A, a base oxide film 402, an island-like crystalline semiconductor (e.g., a silicon semiconductor) region 403, a silicon oxide film 404, and a gate electrode 405 comprising an aluminum film (2,000 Å to 1 μm in thickness) are formed on a substrate 401 having an insulating surface (e.g., a Corning 7059). A porous anodic oxide film 406 is formed at a thickness of 6,000 Å on the upper portion and both sides of the gate electrode (Fig. 7B). The anodic oxidation is effected under the same conditions as those employed in the case of forming the anodic oxide 107. Furthermore, a barrier anodic oxide 407 is formed between the gate electrode 405 and the anodic oxide 406 (Fig. 7C). Then, the silicon oxide film 404 is etched using the anodic oxide 406 as the mask to form a gate insulating film 404' (Fig. 7D).

The anodic oxide 406 is etched thereafter to expose the edge portion of the gate insulating film 404' for a width y (about 6,000 Å). An N-type impurity is introduced into the active layer by ion doping at a dose of 5×10^{14} to 5×10^{15} cm^{-2} and at an accelerating energy of 10 to 30 keV. By thus setting the accelerating voltage to a low value, the N-type impurity can be mostly excluded from the regions 409 and 410 because the gate insulating film functions as a barrier, but it can be introduced into the regions 408 and 411 at a sufficiently high quantity. Phosphine (PH_3) is used as the doping gas. Diborane (B_2H_6) can be used for forming a P-type impurity region.

Nitrogen ions are introduced into the active layer at a dose of 1×10^{14} to 3×10^{16} cm^{-2}, for example, 2×10^{15} cm^{-2} and at an accelerating voltage of 50 to 100 kV, for example, 80 kV. As a result, almost no nitrogen is introduced into the regions 408 and 411, but nitrogen is introduced into the regions 409 and 410 at a concentration of 5×10^{19} to 2×10^{21} atoms·cm^{-3} depending on the depth. The low resistance regions 408 and 411 and the high resistance regions 409 and 410 are formed by difference of the

concentration of the N-type impurity and that of the nitrogen ions. A silicon nitride film 412 is deposited thereafter by plasma CVD at a thickness of 200 to 2,000 Å, for example, 1,000 Å (Fig. 7E).

A XeF excimer laser (a wavelength of 355 nm and a pulse width of 40 ns) is irradiated to activate the impurities thus introduced. The energy density is 200 to 400 mJ/cm², preferably, 250 to 300 mJ/cm². Preferably, the substrate is heated at 200 to 500 °C upon irradiating the laser. Otherwise, lamp annealing by the irradiation of a visible light or a near infrared light can be effected.

Then, as shown in Fig. 7F, a silicon oxide film is formed by CVD at a thickness of 6,000 Å as an interlayer dielectric 414. An interconnection-electrodes 415 and 416 using a multilayered film of aluminum and titanium nitride are formed after forming the contact hole to complete a TFT.

In the present invention, a silicon nitride film is formed by incorporating a gate insulating film 404' on the high resistance region 410. Accordingly, mobile ions such as sodium ions can be prevented from intruding the active layer. since a silicon nitride film traps a positive charge, the semiconductor device according to the present invention prevents a P-type parasitic channel from forming due to the negative charge trapped by the gate insulating film 404' on the high resistance region 410. As a result, a TFT having an excellent frequency characteristics and which is less affected by hot carrier deterioration even with high drain voltage can be obtained.

The silicon nitride film traps a positive charge, but has no effect on trapping a negative charge. Thus, the silicon nitride film is used in an N-channel TFT but not in a P-channel TFT. Preferably, an aluminum nitride or an aluminum oxide is used in a P-channel TFT.

In the present invention, the high resistance region into which oxygen, nitrogen, carbon, and the like are introduced can be

formed in a self-alignment. Because the width of the high resistance region can be determined by an anodic oxide whose thickness can be precisely controlled. By further forming a silicon nitride film either directly or indirectly on the high resistance region, positive charges can be trapped in the silicon nitride film. Thus, the hot carrier effect can be suppressed by the hot carriers which cancel the negative charge trapped in the gate insulating film (silicon oxide).

In case of fabricating a three dimensional integrated circuit by forming the TFT according to the present invention on a substrate having thereon a semiconductor integrated circuit, the TFT is formed on an insulating surface such as of a glass or an organic resin. The TFT according to the present invention is particularly effective for an electro-optical device such as a monolithic active matrix circuit having the peripheral circuit on a same substrate.

The TFT according to the present invention can be used effectively as, for example, a pixel TFT of an active matrix circuit because it has a low reverse leak current and a high withstand voltage. For a TFT in a driver circuit, on the other hand, a high speed operation is required rather than a low leak current. Accordingly, the TFTs for use in such applications are subjected to a treatment to prevent oxygen, nitrogen, carbon, etc., from intruding into the region of the peripheral circuit.

What is Claimed:

1. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor.

2. A semiconductor device according to claim 1 wherein said semiconductor film comprises crystalline silicon.

3. A semiconductor device according to claim 1 wherein said impurity is selected from the group consisting of phosphorus and boron.

4. A semiconductor device according to claim 1 wherein said gate electrode is located over said semiconductor film.

5. A semiconductor device according to claim 1 wherein said gate electrode comprises a multi-layered structure including first and second layers, each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

6. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor and a distance between the channel forming region and the pair of first regions in said first thin film transistor is within a range of 0.4 to 2 μm.

7. A semiconductor device according to claim 6 wherein said semiconductor film comprises crystalline silicon.

8. A semiconductor device according to claim 6 wherein said impurity is selected from the group consisting of phosphorus and boron.

9. A semiconductor device according to claim 6 wherein said gate electrode is located over said semiconductor film.

10. A semiconductor device according to claim 6 wherein said gate electrode comprises a multi-layered structure including first and second layers, each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

11. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions

in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions of said second thin film transistor are overlapped with the gate electrode of said second thin film transistor and a distance between the channel forming region and the pair of first regions in said first thin film transistor is different from that of said second thin film transistor.

12. A semiconductor device according to claim 11 wherein said semiconductor film comprises crystalline silicon.

13. A semiconductor device according to claim 11 wherein said impurity is selected from the group consisting of phosphorus and boron.

14. A semiconductor device according to claim 11 wherein said gate electrode is located over said semiconductor film.

15. A semiconductor device according to claim 11 wherein said gate electrode comprises a multi-layered structure including first and second layers, each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

16. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having an inverter circuit comprising at least a second and third thin film transistors formed over the substrate for driving said active matrix circuit, at least one of said second and third thin film transistors comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions are overlapped with the gate electrode of said second thin film transistor.

17. A semiconductor device according to claim 16 wherein a width of the par of second regions between the channel forming region and the pair of first regions in said first thin film transistor is within a range from 0.4 to 2 μm.

18. A semiconductor device according to claim 16 wherein a width of the par of second regions between the channel forming region and the pair of first regions in said first thin film transistor is different from that of said second and third thin film transistors.

19. A semiconductor device including at least one thin film transistor, said thin film transistor comprising:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein the pair of second regions are overlapped with the gate electrode of said second thin film transistor.

20. A semiconductor device according to claim 19 wherein said semiconductor film comprises crystal silicon.

21. A semiconductor device according to claim 19 wherein said impurity is selected from the group consisting of phosphorous and boron.

22. A semiconductor device according to claim 19 wherein said gate electrode is located over said semiconductor film.

23. A semiconductor device according to claim 19 wherein said gate electrode comprises a multi-layered structure including first and second layers,

each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

24. A semiconductor device according to claim 19 wherein said impurity is contained in said pair of first regions in a concentration within a range from 1 x 10^{20} to 2 x 10^{21} atoms/cm^3.

25. A semiconductor device according to claim 19 wherein said impurity is contained in said pair of second regions in a concentration within a range from 1 x 10^{17} to 2 x 10^{18} atoms/cm^3.

26. A semiconductor device comprising:

an active matrix circuit having at least one first thin film transistor formed over a substrate; and

a driving circuit having at least one second thin film transistor formed over the substrate for driving said active matrix circuit, each of said first and second thin film transistors containing:

a gate electrode;

a gate insulating film adjacent to the gate electrode; and

a semiconductor film adjacent to said gate insulating film wherein said semiconductor film includes a channel forming region, a pair of first regions containing an impurity for giving one conductivity type thereto with said channel forming region therebetween, and a pair of second regions in which a concentration of said impurity is smaller than that in said first regions wherein said second regions are interposed between said channel forming region and said pair of first regions,

wherein a sheet resistance of the pair of second regions is within a range from 10 to 50 kΩ/square.

27. A semiconductor device according to claim 26 wherein said semiconductor film comprises crystalline silicon.

28. A semiconductor device according to claim 26 wherein said impurity is selected from the group consisting of phosphorus and boron.

29. A semiconductor device according to claim 26 wherein said gate electrode is located over said semiconductor film.

30. A semiconductor device according to claim 26 wherein said gate electrode comprises a multi-layered structure including first and second layers, each of which comprises a material selected from the group consisting of aluminum, tantalum, titanium and silicon.

31. A semiconductor device according to claim 26 wherein a distance between the channel forming region and the pair of first regions in said first thin film transistor is within a range of 0.4 to 5 μm.

32. A semiconductor device according to claim 26 wherein a distance between the channel forming region and the pair of first regions in said first thin film transistor is different from that of said second thin film transistor.

33. A semiconductor device according to claim 26 wherein a sheet resistance of the pair of first regions is within a range from 10 to 50 Ω/square.

34. A semiconductor device according to claim 1 wherein the concentration of said impurity in said first regions is within a range from 1 x 10^{20} to 2 x 10^{21} atoms/cm^3 while the concentration of said impurity in said pair of second regions is within a range from 1 x 10^{17} to 2 x 10^{18} atoms/cm^3.

35. A semiconductor device according to claim 6 wherein the concentration of said impurity in said first regions is with a range from 1 x 10^{20} to 2 x 10^{21} atoms/cm^3 while the concentration of said impurity in said pair of second regions is within a range from 1 x 10^{17} to 2 x 10^{18} atoms/cm^3.

36. A semiconductor device according to claim 11 wherein the concentration of said impurity in said first regions is within a range from 1 x 10^{20} to 2 x 10^{21} atoms/cm^3 while the concentration of said impurity in said pair of second regions is within a range from 1 x 10^{17} to 2 x 10^{18} atoms/cm^3.

ABSTRACT

In a thin film transistor (TFT), a mask is formed on a gate electrode, and a porous anodic oxide is formed in both sides of the gate electrode using a relatively low voltage. A barrier anodic oxide is formed between the gate electrode and the porous anodic oxide and on the gate electrode using a relatively high voltage. A gate insulating film is etched using the barrier anodic oxide as a mask. The porous anodic oxide is selectively etched after etching barrier anodic oxide, to obtain a region of an active layer on which the gate insulating film is formed and the other region of the active layer on which the gate insulating film is not formed. An element including at least one of oxygen, nitrogen and carbon is introduced into the region of the active layer at high concentration in comparison with a concentration of the other region of the active layer. Further, N- or P-type impurity is introduced into the active layer. Accordingly, high resistance impurity regions are formed in both sides of a channel forming region.

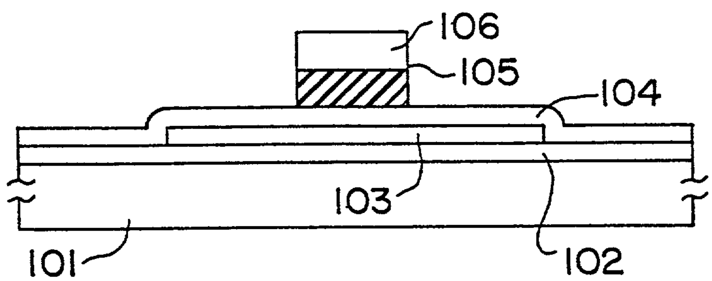

FIG. 1A

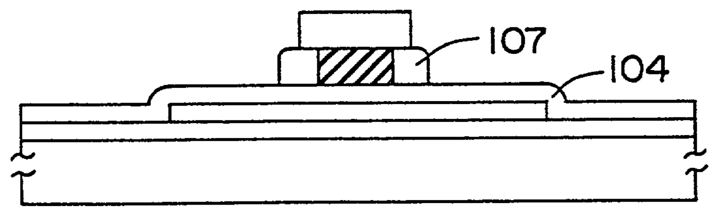

FIG. 1B

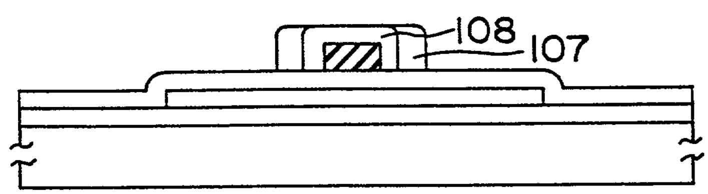

FIG. 1C

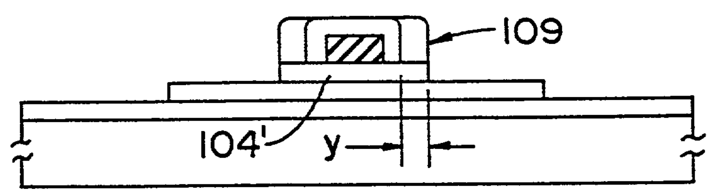

FIG. 1D

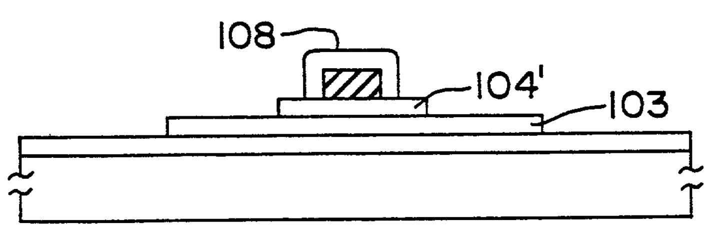

FIG. 1E

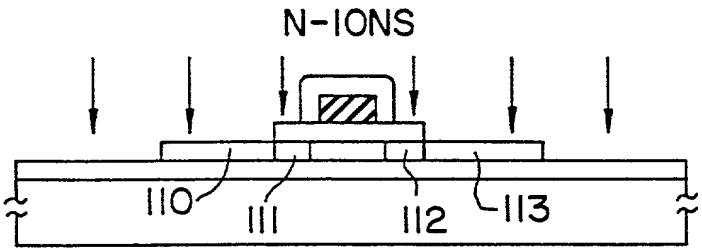

FIG.2A

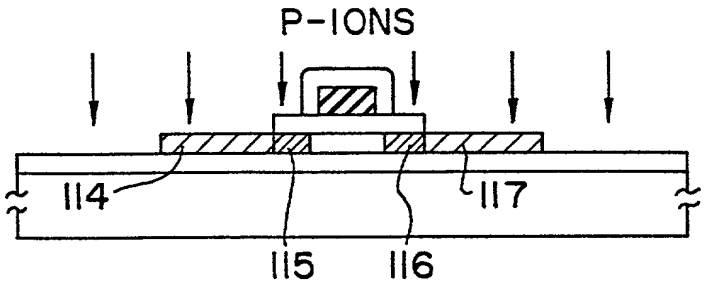

FIG.2B

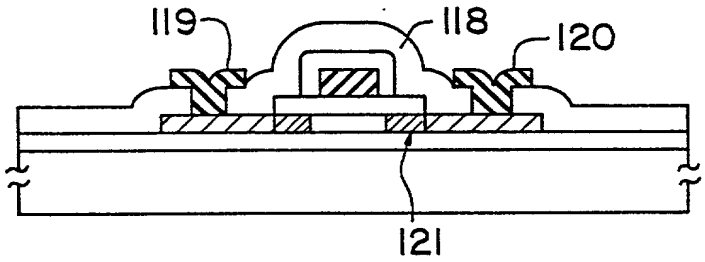

FIG.2C

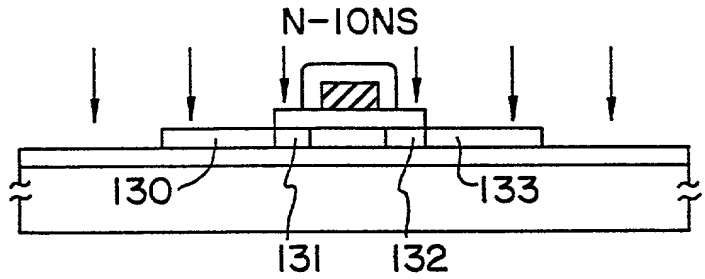

FIG.3A

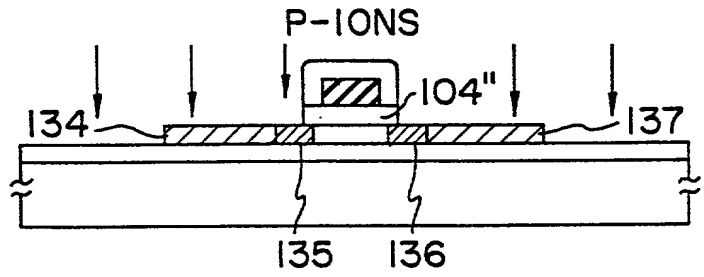

FIG.3B

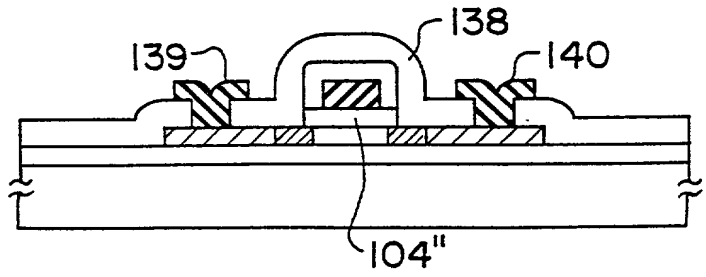

FIG.3C

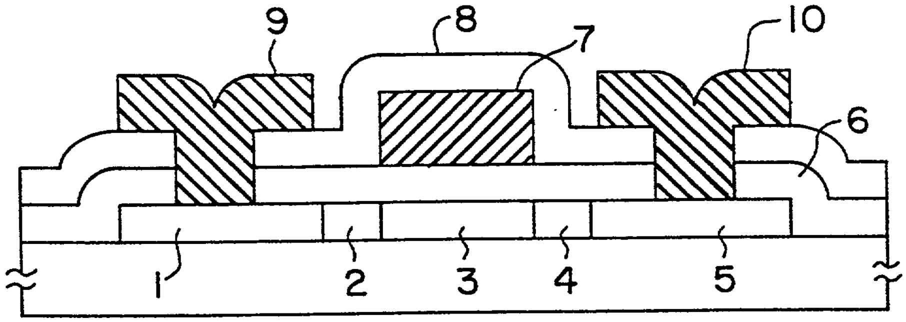

FIG.4A

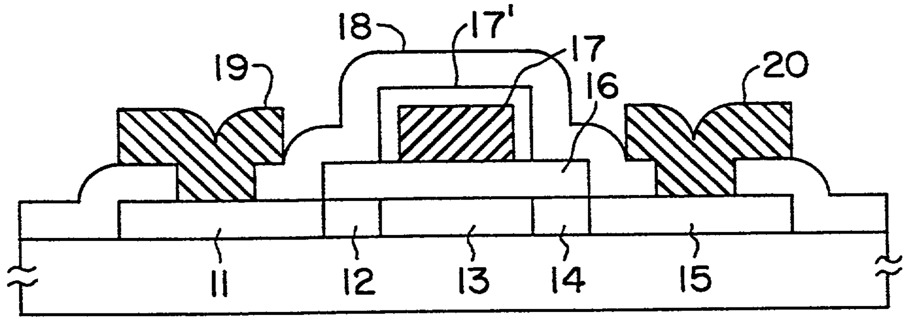

FIG.4B

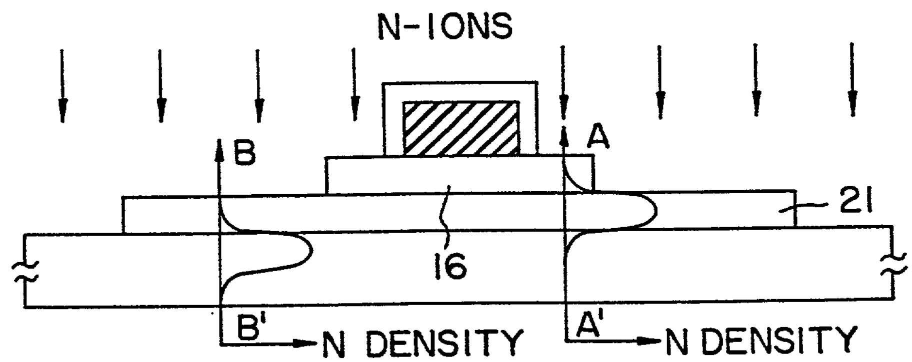

FIG.4C

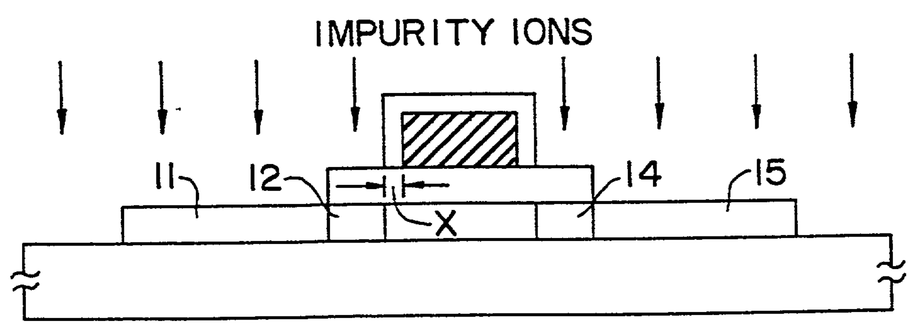

FIG.4D

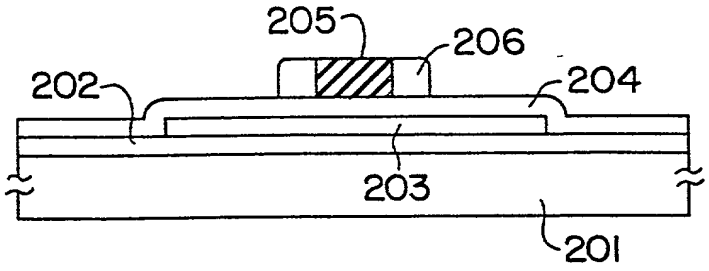

FIG.5A

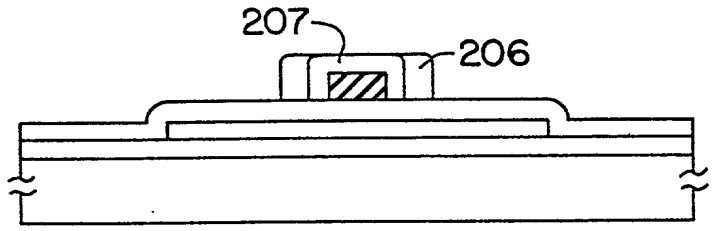

FIG.5B

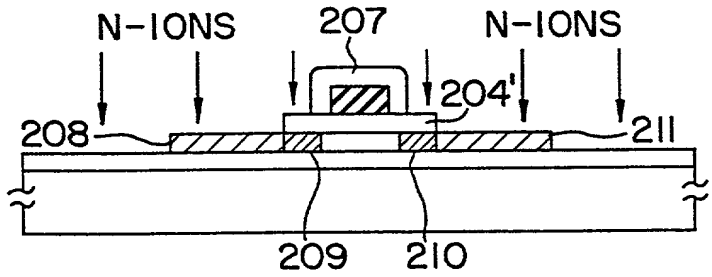

FIG.5C

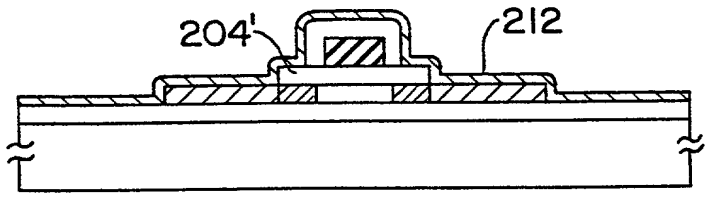

FIG.5D

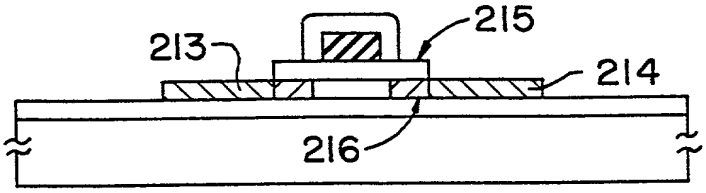

FIG.5E

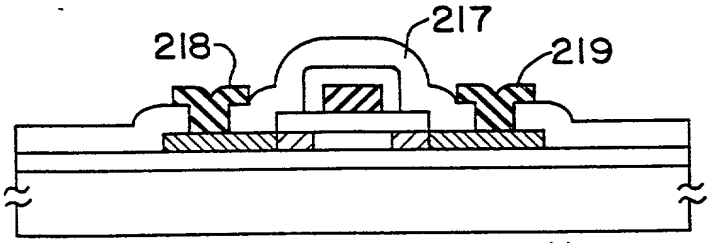

FIG.5F

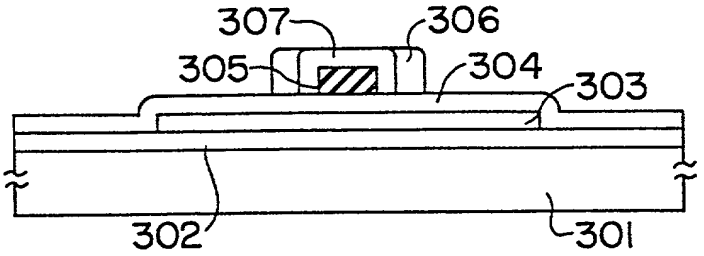

FIG.6A

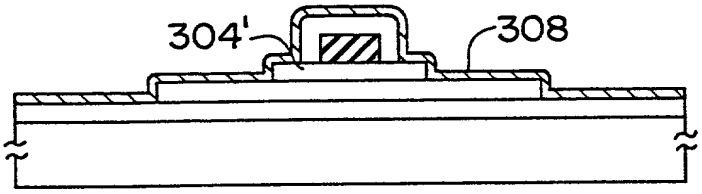

FIG.6B

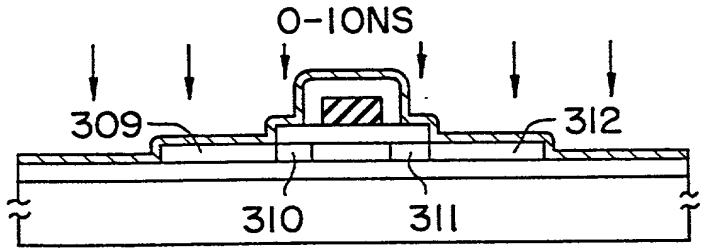

FIG.6C

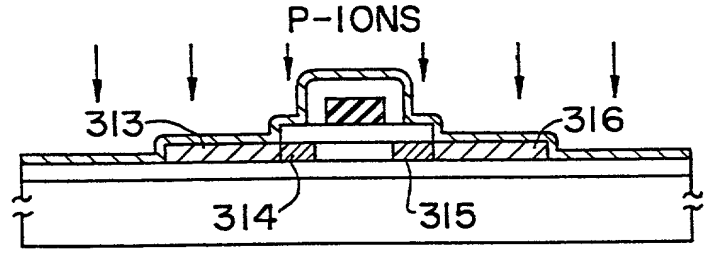

FIG.6D

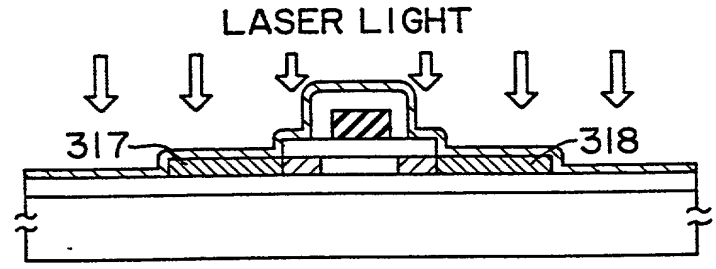

FIG.6E

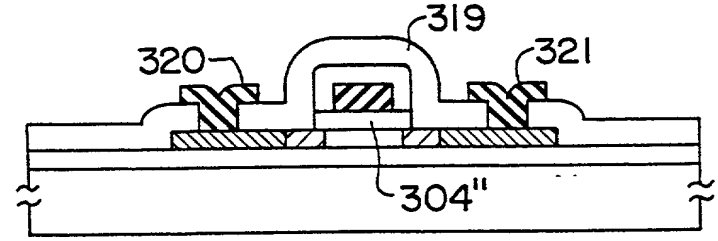

FIG.6F

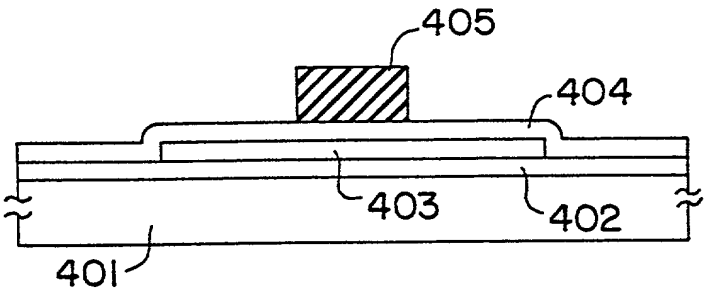

FIG.7A

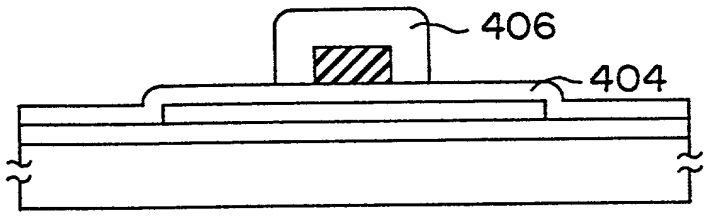

FIG.7B

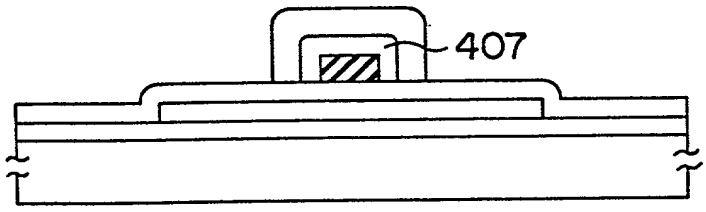

FIG.7C

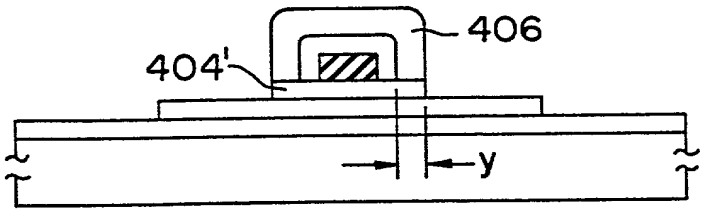

FIG.7D

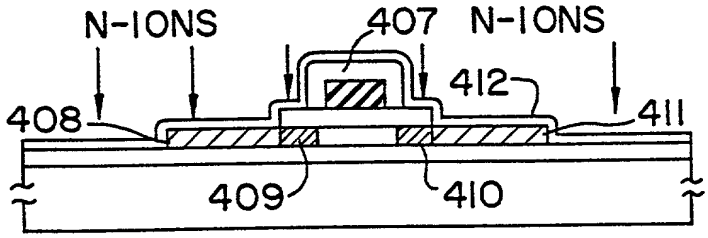

FIG.7E

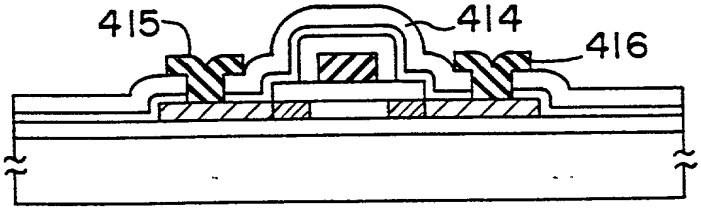

FIG.7F

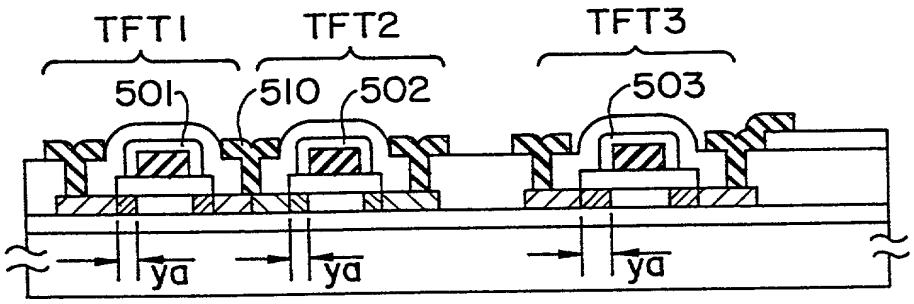
TFT1
TFT2
TFT3
501
510
502
503
ya
ya
ya

FIG.8A

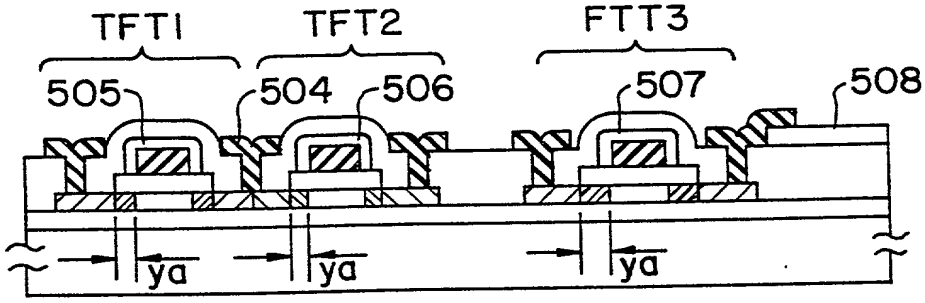
TFT1
TFT2
FTT3
505
504
506
507
508
ya
ya
ya

FIG.8B

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: * Semiconductor Device and Method for Fabricating the Same (Insert Title)

_______________, the specification of which is attached hereto unless the following box is checked:

(Check Box If Appropriate — For Use Without Specification Attached)

☐ The specification was filed on _______________
and was assigned Serial No. _______________ (if known)
and was amended on _______________ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s) — Insert Priority Information (if appropriate)

(Number)	(Country)	(Month/Day/Year Filed)	Priority Claimed Yes	Priority Claimed No
5-269778	JAPAN	October 1, 1993	☒	☐
			☐	☐
			☐	☐
			☐	☐
			☐	☐

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)

Revised 11/90

*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey (Reg. No. 20,932)
Stuart J. Friedman (Reg. No. 24,312)
Charles M. Leedom, Jr. (Reg. No. 26,477)
Gerald J. Ferguson, Jr. (Reg. No. 23,016)
David S. Safran (Reg. No. 27,997)
Thomas W. Cole (Reg. No. 28,290)

Send Correspondence to:

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.
2010 Corporate Ridge, Suite 600
McLean, Virginia 22102
Telephone: (703) 790-9110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Insert Name of Non-U.S. firm, attorney or agent

The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from ______________________ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

Insert Full Name of First or Sole Inventor and Date This Document Is Signed	FULL NAME OF SOLE OR FIRST INVENTOR: Hongyong Zhang	INVENTOR'S SIGNATURE: Hongyong Zhang	DATE: 94.9.22
Insert Residence / Insert Citizenship	RESIDENCE (City, State & Country): Kanagawa, Japan		CITIZENSHIP: Japanese
Insert Post Office Address	POST OFFICE ADDRESS (Complete Street Address including City, State & Country): Paresu Miyagami 302, 1-10-15, Fukamidai, Yamato-shi, Kanagawa-ken 242 Japan		
Second Inventor: see above	FULL NAME OF SECOND JOINT INVENTOR, IF ANY: Hideto OHNUMA	INVENTOR'S SIGNATURE: 大沼英人	DATE: 9-22-94
	RESIDENCE (City, State & Country): Kanagawa, Japan		CITIZENSHIP: Japanese
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country): Flat SEL 306, 304-1, Hase, Atsugi-shi, Kaangawa-ken 243 Japan		
Third Inventor: see above	FULL NAME OF THIRD JOINT INVENTOR, IF ANY: Naoaki YAMAGUCHI	INVENTOR'S SIGNATURE: 山口直明	DATE: Sep. 22, 94
	RESIDENCE (City, State & Country): Kanagawa, Japan		CITIZENSHIP: Japanese
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country): 2737, Shinohara-cho, Kouhoku-ku, Yokohama-shi, Kanagawa-ken 222 Japan		
Fourth Inventor: see above	FULL NAME OF FOURTH JOINT INVENTOR, IF ANY: Yasuhiko TAKEMURA	INVENTOR'S SIGNATURE: [signature]	DATE: Sep 22, '94
	RESIDENCE (City, State & Country): Kanagawa, Japan		CITIZENSHIP: Japanese
	POST OFFICE ADDRESS (Complete Street Address including City, State & Country): Flat Atsugi 208, 931-1, Hase, Atsugi-shi, Kanagawa-ken 243 Japan		